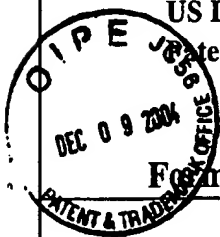|		Atty. Docket No.: 42390.P5193C		Application No.: 09/852,217	

US Department of Commerce
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Form PTO-1449 (Modified)

Atty. Docket No.: 42390.P5193C	Application No.: 09/852,217
Applicant: Abdallah et al.	
Filing Date: May 8, 2001	

US Patent Documents

Examiner's Initials		Date	Document Number	Name	Class	Sub-Class	Filing Date
EC		07/31/90	4,945,479	Rusterholz et al.	712	3	
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EC		09/10/91	5,047,975	Patti et al.	708	706	
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Examiner's Initials		Date	Document Number	Country	Class	Sub-Class	Translation

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

Examiner	Date Considered
[signature]	2/16/05

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US Department of Commerce Patent and Trademark Office	Atty. Docket No.: 042390.P5193C	Application No.: 09/852,217
	Applicant: Abdallah et al.	
Form PTO-1449 (Modified)	Filing Date: May 8, 2001	

US Patent Documents

Examiner's Initials		Date	Document Number	Name	Class	Sub-Class	Filing Date

Foreign Patent Documents

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ЄС	Santoro, Mark; Design and Clocking of VLSI Multipliers. Technical Report No. CSL -TR-89-397, October 1989. Pages i-xii and 1-118.
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Examiner	Eric Colt	Date Considered 2/16/05

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US Department of Commerce Patent and Trademark Office	Atty. Docket No.: 042390.P5193C	Application No.: 09/852,217
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Examiner's Initials		Date	Document Number	Name	Class	Sub-Class	Filing Date

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Examiner *Eric*	Date Considered 2/16/05

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